IN THE SPECIFICATION

Please amend the paragraph starting at page 4, line 28 to read as follows.

In one of its most unusual features, the decoder uses a different mathematical representation internally from that used off-chip for the "Galois field", which is a mathematical structure used in error-correction systems. The importance of this feature is that it makes it possible to easily handle incoming data which may be expressed in a different Galois-field representation from that used internally on the chip, either by minor changes at the gate array level or, in an alternative implementation, by providing programmability on the chip for different representations; furthermore, this feature ~~make~~ makes it possible to choose the representation used on-chip independently of that used for the incoming data so as to optimize speed and gate-count for the chip, specifically by using a novel quadratic-subfield modular multiplier circuit and a novel power-subfield integrated Galois-field division circuit on the chip.

Please amend the paragraph starting at page 13, line 15 to read as follows.

The Chien-Forney circuit 16 is used to implement the Forney algorithm for use with ~~Read-Solomon~~ Reed-Solomon codes with "offsets". The Chien-Forney circuit 16 requires fewer stages for the calculation and can perform at higher speed than conventional Forney-algorithm circuits. The Chien-Forney circuit 16 may be used in a wide variety of applications not limited to the present decoder 10.

Please amend the Abstract of the disclosure as follows.

A programmable error-correction decoder embodied in an integrated circuit and error correction decoding method that performs high-speed error correction for digital communication channels and digital data storage applications. The decoder carries out error detection and correction for digital data in a variety of data transmission and storage applications. The decoder has three basic modules, including a syndrome computation module, a Berlekamp-Massey computation module, and a Chien-Forney module. The syndrome computation module calculates syndromes which are intermediate values required to find error locations and values. The Berlekamp-Massey module implements a Berlekamp-Massey algorithm that converts the syndromes to intermediate results known as lambda (Λ) and omega (Ω) polynomials. The Chien-Forney module uses modified Chien-search and Forney algorithms to calculate actual error locations and error values. ~~The decoder can decode a range of BCH and Reed-Solomon codes and shortened versions of these codes and can switch between these codes, and between different block lengths, while operating on the fly without any delay between adjacent blocks of data that use different codes.~~ Translator and inverse-translator circuits are employed that employ ~~allow optimal choice of the internal on-chip Galois field~~

~~representation for maximizing chip speed and minimizing chip gate count by making possible the use of~~ a novel quadratic-subfield modular multiplier and a novel power-subfield integrated Galois-field divider. ~~A simplified Chien-Forney algorithm is implemented that requires fewer computations to determine error magnitudes for Reed-Solomon codes with offsets compared to conventional approaches, and which allows the same circuitry to be used for different codes with arbitrary offsets.~~

a4